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AMENDMENTS TO THE CLAIMS:

1. (Original) A semiconductor memory device having an error check and correction (ECC) type error recovery circuit comprising:

a memory cell array including at least one normal memory cell array portion and an ECC memory cell array portion, said normal memory cell array portion including a plurality of normal memory cells, and said ECC memory cell array portion including a plurality of ECC memory cells;

an X decoder for selecting one of word lines in said memory cell array, said word lines extending from said X decoder to said memory cell array; and

an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line, said cell data including data from normal cells and ECC cells of said selected word line;

wherein said ECC memory cell array portion is disposed at a location other than the far end of said word lines from said X decoder.

2. (Currently amended) A semiconductor memory device having an error check and correction (ECC) type error recovery circuit comprising:

a memory cell array including at least one normal memory cell array portion and an ECC memory cell array portion, said normal memory cell array portion including a plurality of normal memory cells, and said ECC memory cell array portion including a plurality of ECC memory cells;

an X decoder for selecting one of word lines in said memory cell array, said word lines extending from said X decoder to said memory cell array; and

an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line, said cell data including data from normal cells and ECC cells of said selected word line;

wherein said ECC memory cell array portion is disposed at a location other than the far end of said word lines from said X decoder, and

~~A semiconductor memory device as set forth in claim 1,~~

wherein said ECC memory cell array portion is disposed at a middle portion of said memory cell array.

3. (Currently amended) A semiconductor memory device having an error check and correction (ECC) type error recovery circuit comprising:

a memory cell array including at least one normal memory cell array portion and an ECC memory cell array portion, said normal memory cell array portion including a plurality of normal memory cells, and said ECC memory cell array portion including a plurality of ECC memory cells;

an X decoder for selecting one of word lines in said memory cell array, said word lines extending from said X decoder to said memory cell array; and

an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line, said cell data including data from normal cells and ECC cells of said selected word line;

wherein said ECC memory cell array portion is disposed at a location other than the far end of said word lines from said X decoder, and

~~A semiconductor memory device as set forth in claim 1,~~

wherein said ECC memory cell array portion is disposed substantially at the central portion of said memory cell array.

4. (Original) A semiconductor memory device as set forth in claim 1, wherein said ECC memory cell array portion is disposed at the near end of said word lines on the side of said X decoder.

5. (Original) A semiconductor memory device as set forth in claim 1, wherein said at least one normal memory cell array portion comprises a plurality of normal memory cell array portions.

6. (Original) A semiconductor memory device as set forth in claim 1, further comprising a Y decoder and digit lines extending from said Y decoder toward said memory cell array.

7. (Original) A semiconductor memory device as set forth in claim 1, wherein said cell data is supplied to said ECC operation circuit via sense amplifiers.

8. (Previously presented) A semiconductor memory device as set forth in claim 1, wherein said semiconductor memory device comprises a random access memory (RAM) device.

9. (Previously presented) A semiconductor memory device as set forth in claim 1, wherein said semiconductor memory device comprises a read-only memory (ROM) device.

10. (Original) A semiconductor memory device as set forth in claim 1, wherein data read out from said normal memory cell array portions can be outputted to outside of said semiconductor memory device without undergoing ECC operation by said ECC operation circuit.

11. (Original) A semiconductor memory device having an error check and correction (ECC) type error recovery circuit comprising:

a memory cell array including a plurality of normal memory cell array portions and an ECC memory cell array portion, each of said normal memory cell array portions

including a plurality of normal memory cells, and said ECC memory cell array portion including a plurality of ECC memory cells;

an X decoder for selecting one of word lines in said memory cell array, said word lines in said memory cell array, said word lines extending from said X decoder to said memory cell array;

a Y decoder and digit lines extending from said Y decoder toward said memory cell array;

an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line, said cell data including data from normal cells and ECC cells of said selected word line;

wherein said ECC memory cell array portion is disposed at a location other than the far end of said word lines from said X decoder.

12. (Original) A semiconductor memory device as set forth in claim 11, wherein said ECC memory cell array portion is disposed at a middle portion of said memory cell array.

13. (Previously presented) A semiconductor memory device as set forth in claim 11, wherein said ECC memory cell array portion is disposed substantially at the central portion of said memory cell array.

14. (Original) A semiconductor memory device as set forth in claim 11, wherein said ECC memory cell array portion is disposed at a near end of said word lines on the side of said X decoder.

15. (Previously presented) A semiconductor memory device as set forth in claim 1, wherein sad ECC memory cell array portion is disposed at a location other than the far end and a near end of said word lines from said X decoder.

16. (Previously presented) A semiconductor memory device as set forth in claim 1, wherein sad ECC memory cell array portion is disposed at a location on said word lines between locations of at least two of the plurality of normal memory cells on said word lines.

17. (Previously presented) A semiconductor memory device as set forth in claim 11, wherein a selection time of said ECC memory cells in said ECC memory cell array portion is less than a selection time of at least one of the plurality of normal memory cells in said normal memory cell array.

18. (Previously presented) A semiconductor memory device as set forth in claim 1, wherein a read out speed of data from said ECC memory cells in said ECC memory cell

array portion is less than a read out speed of at least one of the plurality of normal memory cells in said normal memory cell array.

19. (Previously presented) A semiconductor memory device as set forth in claim 11, wherein said ECC memory cell array portion is disposed at a location on said word lines for limiting a time for selecting said ECC memory cells in said ECC memory cell array portion to a time that is less than a time for selecting at least one of the plurality of normal memory cells in said normal memory cell array.

20. (Previously presented) A semiconductor memory device as set forth in claim 11, wherein said ECC memory cell array portion is disposed at a location on said word lines for limiting a read out speed of data from said ECC memory cells in said ECC memory cell array portion to a read out speed that is less than a read out speed of at least one of the plurality of normal memory cells in said normal memory cell array.